Performance Optimization of GaN-Based FinFETs: Impact of Fin Width on Electrical Characteristics and Device Efficiency

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ABSTRACT: GaN-based materials, a third-generation semiconductor, provide high breakdown field strength and mobility, enhancing system performance and reducing integration costs with GaN CMOS technology. Fin structure, combined with GaN's advantages, improves gate control and reduce short channel effects, which offers superior performance for high power and high frequency applications. In this paper, Fin technology is investigated through TCAD simulations across different channel widths (Wfin), we analyzed the threshold voltage (Vth), subthreshold swing (SS), saturation current, and transconductance. The physical insights of these trends were further elucidated through the analysis of electric field and current density distributions within the channel at saturation.

01 Introduction

As a third-generation semiconductor material [1], GaN-based materials exhibit high breakdown field strength, high saturation electron velocity, and high mobility two-dimensional electron gas due to GaN-based heterojunctions. GaN complementary metal oxide semiconductor (CMOS) technology, integrating the n-FET and p-FET GaN, not only improves performance at the system level, but also reduces the cost during monolithic integration [2].

In traditional MOSFET as the device size shrinks, the drain potential has a stronger influence on the gate control ability, leading to short channel effect, resulting in the rise of the take-off drain current, the degradation of subthreshold characteristics and the generation of the source leakage through effect, which deteriorates the device performance[3]. FinFET structure enhances the gate control ability by increasing the gate dimension to achieve the suppression of the short channel effect. GaN-based FinFET combines the material advantages of GaN and the special structure of Fin, which offers it significant advantages in high power and high frequency applications

02 Research Purpose

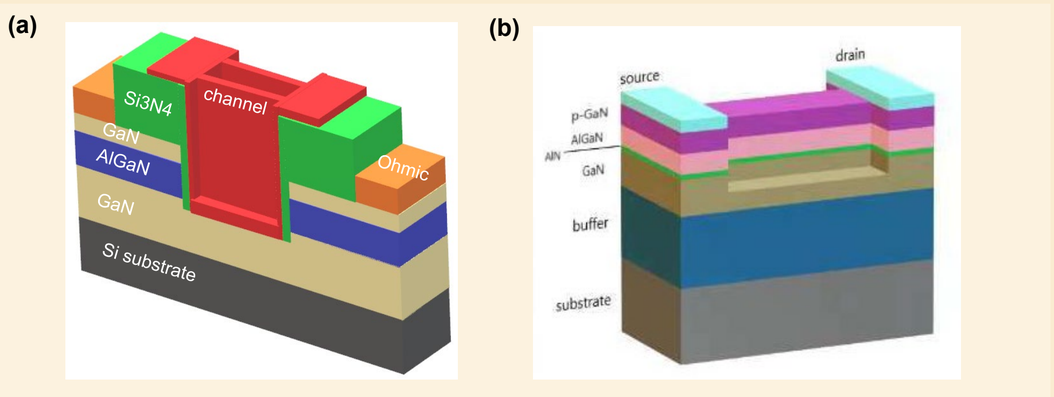

Fig. 1. Structures of (a) n-type FinFET and (b) p-type FinFET devices.

This paper mainly aims to investigate fin technology and its performance in (1) normally-ON, normally-OFF operation, (2) gate controllability, (3) linearity, gm, and diminished short channel effect. GaN-based FinFET structure is demonstrated in figure 1. This paper mainly focuses on simulating the n-channel FinFET structure through sentauraus TCAD and analyzing transfer, output characteristics curve, electric field distribution, and current density of the structure with different fin widths.

03 Methodology

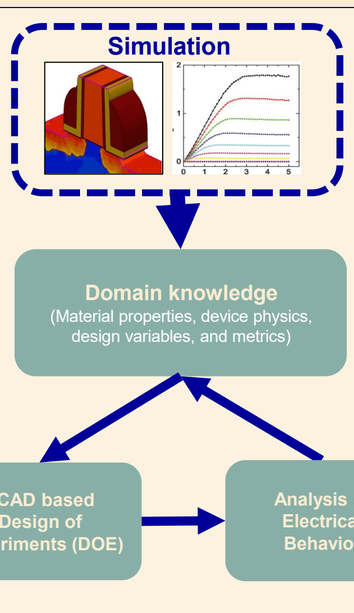
Simulation
Domain knowledge
(Material properties, device physics, design variables, and metrics)
TCAD based Design of Experiments (DOE)
Analysis of Electrical Behavior

Fig. 2. (a) work flow for transistor design and optimization

The steps required for device design and simulation include:

1. **Device Specification:** Figure of merit (FOM) derived from application requirements.
2. **Preliminary Device Geometry:** Leverage domain knowledge to identify initial device architecture and key design variables.
3. **Design of Experiments (DOE):** Generate design variable splits for device optimization using DOE.
4. **Analysis of Electrical Data:** Analyze results to uncover variable correlations and guide design.

This process involves various TCAD modules, requiring an integrated TCAD environment for efficient design as shown in fig. 2. (b).

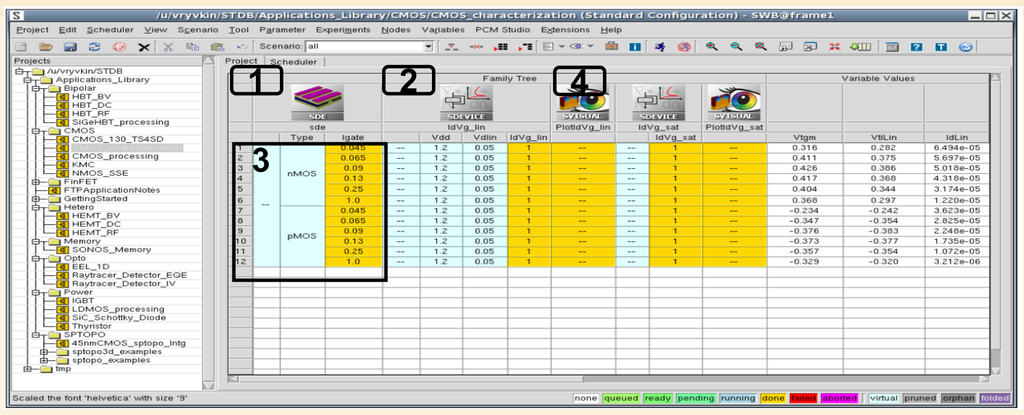

Fig. 2. (b) Integrated TCAD Environment (Workbench)

04 Device Simulation Results

A. Threshold Voltage (Vth) and Subthreshold Swing (SS):

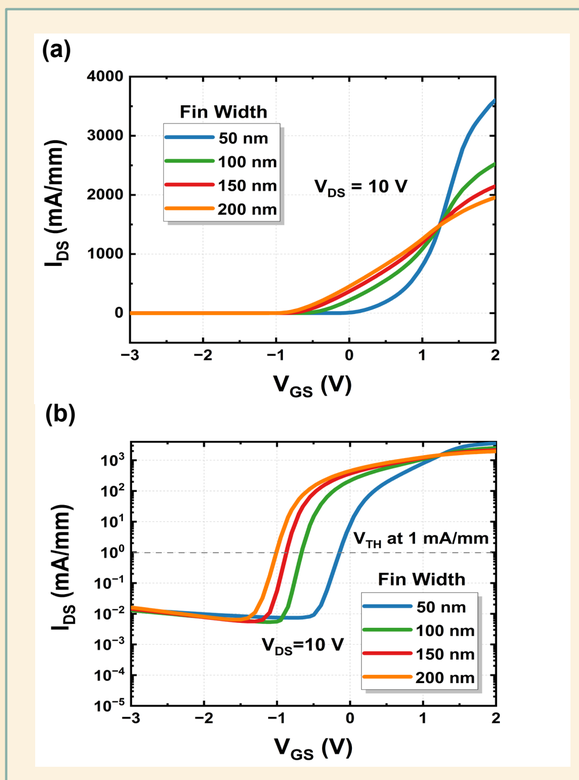

Fig. 3. Transfer characteristics of n-type Fin in (a) linear scale; (b) log scale.

As Wfin decreases, Vth progressively increases and shifts positively, primarily due to stronger gate control and depletion region expansion in narrower fins. The enhanced electrostatic control of the gate over the channel leads to more effective depletion, requiring a higher gate voltage to form a conductive channel. Additionally, the overlapping depletion regions in narrower fins cause the channel to fully deplete at lower voltages, further increasing Vth. The decrease in SS with narrower channels further confirms this enhanced gate control.

B. Saturation Current and Transconductance

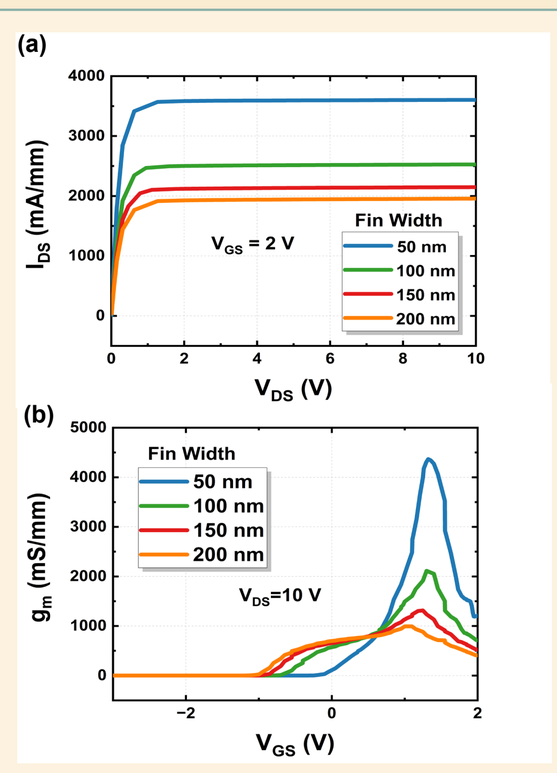

Fig. 4. (a) Output characteristics of n-type Fin in linear scale; (b) .

With decreasing Wfin, the saturation current increases, indicating better current driving capability in narrower channels. The peak transconductance (gm) also rises with decreasing channel width, attributed to the enhanced control over channel charges from the top and side gates, which increases intrinsic gate capacitance and improves transconductance.

C. Electric Field Distribution and Current Density

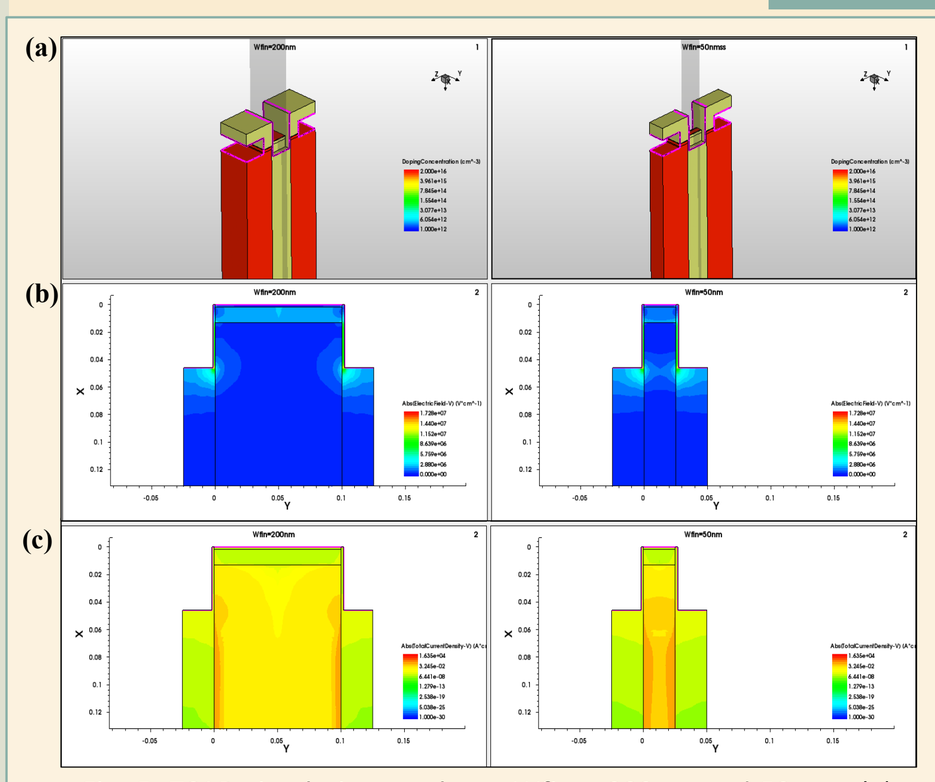

Fig. 5. TCAD simulation results at Wfin = 200nm and 50 nm: (a) TCAD cross-section profile (b) Electric Field Distribution; (c) Current Density.

In the 200 nm Wfin device, current is primarily concentrated at the top of the channel, with relatively lower current density at the sidewalls and bottom, indicating weaker gate control over these regions. In contrast, in the 50 nm device, the current density is more uniformly distributed across the cross-section of the Fin, with higher current density observed. This suggests that the gate can more effectively control the entire channel region, leading to more concentrated current flow throughout the fin structure.

04 CONCLUSION

The investigation of GaN-based FinFETs shows significant performance improvements with narrower fin widths. Reducing fin width (Wfin) enhances key metrics such as threshold voltage (Vth), subthreshold swing (SS), saturation current, and transconductance (gm) by improving gate control and mitigating short-channel effects. Narrower fins (50 nm) offer better electric field distribution and current density compared to wider fins (200 nm), highlighting their potential for high power and high frequency applications. This underscores the benefits of adopting narrower fin technologies for advanced GaN-based semiconductor devices.

05 REFERENCE

[1] N. Chowdhury, Q. Xie, and T. Palacios, 'Self-Aligned E-Mode GaN p-Channel FinFET With ION > 100 mA/mm and ION/IOFF > 107'.
[2] H. Du et al., 'High-Performance E-Mode p -Channel GaN FinFET on Silicon Substrate With High I ON / I OFF and High Threshold Voltage', IEEE Electron Device Lett., vol. 43, no. 5, pp. 705–708, May 2022, doi: 10.1109/LED.2022.3155152.
[3] Zhang, Y., Zubair, A., Liu, Z., Xiao, M., Perozek, J., Ma, Y., & Palacios, T. (2021). GaN FinFETs and trigate devices for power and RF applications: review and perspective. Semiconductor Science and Technology, 36(5), 054001. https://doi.org/10.1088/1361-6641/abde17